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328454(28)

B. E. (Fourth Semester) Examination, April-May 2020

(New Scheme)

(Et & T Branch)

MICROPROCESSOR and INTERFACES

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *All questions are compulsory and carry equal marks. Part (a) of each question is compulsory. Attempt any* ***two*** *parts from (b), (c) and (d) of each question.*

Unit-I

1. (a) Define Instruction Cycle. How many T-states required in an instruction cycle to execute CALL addr (16) instruction? 2

(b) Draw circuit using 3 : 8 decoder to generate memory and IO control signals for read / write operation. Why 04 outputs of 3 : 8 decoder are invalid in this case? 7

(c) Draw and explain step by step timing diagram for the instruction 'JNZ lable' if the condition is not satisfied. 7

(d) Explain the process of demultiplexing of Address data bus AD_0 - AD_7 using timing diagram. 7

Unit-II

2. (a) List any four instructions to clear Accumulator. 2

(b) Write function of following instructions. Also list number of machine cycles, no. of T-states and number of bytes for the instruction. 7

(i) LDAX B
(ii) XTHL
(iii) PUSH PSW
(iv) SHLD address (16 bit)

(c) Define assembler directives. List different assembler directives used in 8085 microprocessor and explain function of any four directives. 7

(d) Write an assembly language program to generate a time delay using two registers. If the two registers consist of data P and Q, write an expression for time delay produced. 7

Unit-III

3. (a) If the number of address lines for a memory ROM is 14, determine the size of memory in KB. 2

(b) Explain peripheral controlled data transfer scheme. 7

(c) Draw and explain, how decoding circuit is designed using NAND gate and using 3 : 8 decoder in case of full decoding technique. 7

(d) Design a memory system for 8085 microprocessor using memory modules 8 KB ROM, 4 KB EPROM and 2 KB of RAM. Let the starting address of 8 KB ROM is 4000 H. Assign addresses to EPROM and RAM such that no address space loss occure in resulting memory map. Use absolute decoding technique for interfacing. 7

Unit-IV

4. (a) Define maskable interrupts, with examples. Which instructions are used to enable or disable such interrupts? 2

(b) Define software interrupts. List all the software interrupts alongwith their Hex-code and vector addresses. Draw the hardware to generate hex-codes for such interrupts. 7

(c) Explain interrupt process when an appropriate signal is applied on INTR pin of microprocessor. 7

(d) Write a SIM word to enable RST 7·5, RST 6·5 and RST 5·5 interrupts. Write a program to get the byte from an input port (with address 80 H), compliment it and send to the output port (with address 81 H), whenever an interrupt occure on RST 7·5. 7

Unit-V

5. (a) What is the basic difference between : 2

(i) 8155 and 8156

(ii) 8355 and 8755

(b) Explain timer operation of 8155 with example. 7

(c) Write control word for simple I/O and BSR mode of 8255. Explain bitwise function. 7

(d) Draw and explain internal architecture of 8259 A. 7